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|---|---|
| PROCTOR, JASON SCOTT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2123 | |

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/854,491 | HOULIHANE ET AL. | |
| | Examiner | Art Unit | |
| | Jason Proctor | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

In the previous Office Action, claims 1-43 were rejected. Applicants' response of 14 November 2005 has amended claims 1, 17, 18, 32-35, 40, 42, and 43 and added new claims 44-49. Claims 1-49 have been rejected.

The Examiner apologizes for the organization of the previous Office Action, but respectfully submits that it was fully responsive to Applicants' previous reply. The present Office Action will be drafted with a typical organization. If Applicants have difficulty in understanding the substance of an Office Action, Applicants are encouraged to contact the Examiner at the phone number provided in the Conclusion.

### *Specification*

The previous objection to the specification for the use of trademarks has been withdrawn in response to Applicants' amendments to the specification.

### *Claim Rejections – 35 USC § 101*

The previous rejections under 35 U.S.C. § 101 of claims 18, 33, and 42 have been withdrawn in response to Applicants' amendments.

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claims 34 and 43 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claims 34 and 43, the limitations recite an intangible data abstraction and define descriptive material *per se*. Please see MPEP 2106(IV)(B)(1)(b). The amendments to claim 34 to recite that the "reduced hardware model [is] embodied in hardware" do not overcome the grounds for this rejection. The "model" of these claims is merely an arrangement of data, thus nonfunctional descriptive material.

In response, Applicants argue primarily that:

> Claims 34 and 43 have both been amended to recite that in claim 34 the reduced hardware model is "embodied in hardware" and that the "reduced model comprises software." As a result, the amended language is believed clearly statutory.

The Examiner respectfully traverses this argument as follows.

Inasmuch as the "model" of claims 34 and 43 refer to a nonfunctional arrangement of data, reciting that the data structure is "embodied in hardware" does not render that data statutory. As stated in MPEP 2106 (IV)(B)(1),

> "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.

And

> In the final analysis under 101, the claimed invention, as a whole, must be evaluated for what it is.") (quoted with approval in *Abele*, 684 F.2d at 907, 214 USPQ at 687). See also *In re Johnson*, 589 F.2d 1070, 1077, 200 USPQ 199, 206 (CCPA 1978) ("form of the claim is often an exercise in drafting"). Thus, nonstatutory music is not a computer component and it does not become statutory by merely recording it on a compact disk.

To overcome the basis for this rejection, the "model" must not fall into this category of nonfunctional descriptive material.

***Claim Rejections - 35 USC § 112***

The previous rejections under 35 U.S.C. § 112, first and second paragraphs, have been withdrawn in response to Applicants' amendments.

***Claim Rejections – 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 12-14, 16-21, 28-30, 32-34, 35-37, and 41-43 are rejected under 35 U.S.C. § 102(b) as being anticipated by Gupte et al., US Patent No. 5, 903, 475 (Gupte).

Regarding claim 1, Gupte discloses a method for simulating circuits wherein

Conducting a simulation of a data processing apparatus performing a test sequence of data processing operations [*"generating a programming language capture module that captures inputs to and outputs from the integrated circuit during system simulation,"* (column 2, lines 23-33)],

including simulating operation of both a subsystem under test and one or more surrounding circuits [*"system simulation"* (column 2, lines 2-22); also (column 9, lines 22-34; column 9, lines 22-34)] where a system simulation is equivalent to testing a subsystem under test in conjunction with the surrounding components that comprise the system,

recording, in response to a change, input signals to and output signals from said subsystem circuit while performing said test sequence of data processing operations [*"The*

*Vector Capture program generates the capture module which is an HDL file that is utilized during a system simulation to capture the input and output vectors around the ASIC."* (column 10, lines 6-9); *"At step 462, the system generates code to capture outputs on each strobe edge. The system generates code to open a single input file and one output file for each output. At step 466, the system generates code to capture inputs on change and the capture module has been generated."* (column 10, lines 25-29); also (column 2, lines 7-22; column 6, lines 53-64; column 9, lines 18-21)];

using at least representation of recorded input signals to form a reduced model to replay recorded input signals to subsystem circuit model and to apply a plurality of sampling rules to said output signals to sample said output signals to detect changes and times of changes in said output signals and to compare said output signals with at least one predetermined characteristic indicative of correct operation [*"The stand-alone simulation generates output test vectors 366. Verifying the representation of the ASIC entails comparing the "golden" vectors to the test vectors. If the golden and test vectors are identical, then the representation of the ASIC used during stand-alone simulation is the same as the customers original behavioral model."* (column 9, lines 30-41); also (column 2, lines 7-22; column 6, lines 41-52); regarding sampling rules, see (column 8, line 49 – column 9, line 8)];

whereby a subsystem under test and reduced model may be used to simulate the subsystem under test performing the test sequence of data processing operations without simulating operation of one or more surrounding circuits [*"Thus, the customer's system simulation is reproduced without having to reproduce the customer's system environment which*

*allows the operation of the ASIC to be verified during various states of synthesis."* (column 8, lines 36-40); also (column 2, lines 7-22; column 6, lines 41-64)].

In response, Applicants' argue primarily that:

> A difference between the present invention and known system for modeling data processing systems is that in accordance with the present invention, input and output signals **are not sampled periodically**, but instead are recorded in response to the change in those signals.

The Examiner respectfully submits that the language of claim 1 recite, *inter alia*, "Recording, in response to a change, input signals to and output signal" but does not expressly recite recording in response to the change **in those signals**. According to the language of the claim, the change could be, for example, a periodic strobe or clock signal.

The Examiner submits that Applicants' argument appears to accurately identify a potential deficiency in the Gupte reference, however the corresponding distinction is not precisely reflected in the claim language.

As per Applicants' request, the following specifically points out how Gupte meets the claim language.

[*"The Vector Capture program generates the capture module which is an HDL file that is utilized during a system simulation to capture the input and output vectors around the ASIC."* (column 10, lines 6-9); *"At step 462, the system generates code to capture outputs on each strobe edge. The system generates code to open a single input file and one output file for each output. At step 466, the system generates code to capture inputs on change and the capture module has been generated."* (column 10, lines 25-29); also (column 2, lines 7-22; column 6, lines 53-64; column 9, lines 18-21)]

Applicants' submit analogous arguments for claim 17, 19, 32, 35, 40, 41 and 44, which have been addressed above.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 2, Gupte discloses the use of a configuration file including data specifying input signals, output signals, and bi-directional signals exchanged with the subsystem circuit in order to form the reduced model [*"bidirect enable definitions"* (column 8, line 44 – column 9, line 8)].

Regarding claim 3, Gupte discloses that signals from the subsystem are used to determine when bi-directional signals can be driven making allowance for variations in delays inherent in output loads [*"The input and output for an inout are combined using the associated BDENABLE signal which specifies whether the inout is an input or an output. Code is generated that assigns the inout to the input wire or the output wire depending on the value of the input test signal."* (column 10, lines 11-17)].

Regarding claim 4, Gupte discloses that the reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation [*"The strobes section specify the appropriate time to capture expected vectors. In the sample IOS file, all outputs are assumed to be synchronous and periodical such that the line 'strobe strb1 period 20 start 19 stop 0 outputs*

*pout dav dbus' will instruct the simulators to extract output vectors every 20 ns on the signals pout, dav and dbus starting 19 ns into the cycle."* (column 8, line 44 – column 9, line 8)].

Regarding claim 5, Gupte discloses recording output signals from a subsystem circuit under test (column 8, line 44 – column 9, line 8). While Gupte et al. does not explicitly disclose that the output signals values are one of: high; low; changed; and high impedance, it is inherent that signals in a digital circuit are referred to by the values in the enumerated group or by equivalent terms. Therefore, by recording output signals, the invention of Gupte records values which are one of: high; low; changed; and high impedance.

Regarding claim 12, Gupte discloses that the full subsystem circuit model from which said input signals and said output signals are recorded may be different from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed [*"During system simulation, the invention captures 'golden' vectors that may be used to test the ASIC during stand-alone simulation... Thus, the customer's simulation system is reproduced without having to reproduce the customer's system environment which allows the operation of the ASIC to be verified during various states of synthesis."* (column 2, lines 7-22); *"The stand-alone simulation reproduces the customers system simulation without having to reproduce the customer's system environment."* (column 9, lines 22-34)].

Regarding claim 13, Gupte discloses that the full subsystem circuit model may change between different versions during regression testing [*"The design configuration managers*

*maintain versions of the design information and security for modification of the design information."* (column 17, lines 14-25); *"The system then issues a command to check out the HDL code for the requested design version from the design configuration manager at step 1002."* (column 18, lines 19-24)].

Regarding claim 14, Gupte discloses that the full subsystem circuit may change between being one of an RTL model, a netlist model, or other software views [*"Additionally, the Capture may be utilized to test the generation of a gate level model from an RTL model... The outputs are compared to verify that the gate level model is an accurate depiction of the ASIC."* (column 9, lines 42-46)].

Regarding claim 16, Gupte discloses recording progress messages for replay during regression testing [*"The system prints statistics at step 414."* (column 9, line 58 – column 10, line 4)]. Statistics are presumed equivalent to progress messages.

Regarding claim 17, the limitations recite an apparatus which performs the method as recited by claim 1. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7), the limitations of claim 17 are rejected by reasoning similar to that used to reject the limitations of claim 1 above.

Regarding claim 18, the limitations recite a computer program product comprising a computer program for controlling a computer to perform a method as recited in claim 1. As the

invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7), the limitations of claim 18 are rejected by reasoning similar to that used to reject the limitations claim 1 above.

Regarding claims 19, 20-21, and 28-30, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claims 4-5 and 12-14. As the invention of Gupte models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the limitations of claims 19, 20-21, and 28-30 are rejected by reasoning similar to that used to reject claims 1, 4-5, and 12-14 above.

Regarding claim 32, the limitations recite an apparatus for modeling a data processing apparatus corresponding to the apparatus for creating a model of a data processing apparatus as recited in claim 17. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) and performs a simulation of the data processing apparatus (column 1, lines 62-65; column 2, lines 7-22) the limitations of claim 32 are rejected by reasoning similar to that used to reject the limitations of claim 17 above.

Regarding claim 33, the limitations recite a computer program product comprising a computer program controlling a computer to perform a method as claimed in claim 19. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of claim 33 are rejected by reasoning similar to that used to reject the limitations of claim 19 above.

Regarding claim 34, Gupte discloses a reduced hardware model embodied in hardware synthesised from a reduced model, wherein the reduced model comprises software [*"[T]he behavioral specification of the ASIC is simulated within the customer's system environment... During the simulation of step 208, the invention captures "golden" vectors that are used to test the ASIC during stand-alone simulation... Thus, the customer's system simulation is reproduced without having to reproduce the customer's system environment which allows the operation of the ASIC to be verified during various states of synthesis described below. Additionally, the test bench for testing the ASIC in stand-alone simulation is automatically generated thereby eliminating the need ofr the user to generate a test bench."* (column 6, lines 48-64).

Claim 35 recites a combination of limitations found in claims 1 and 4 and is rejected for similar reasons to those given above for claims 1 and 4.

Claims 36 and 37 recite combinations of limitations found in claims 5 and 3, respectively, and are rejected for similar reasons to those above for claims 5 and 3.

Claim 41 recites an apparatus that performs the method of claim 1. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of claim 43 are rejected by reasoning similar to that used to reject the limitations of claims 1 and 4 above.

Claim 42 recites a computer program product that performs the method of claim 35. As the invention of Gupte is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of

claim 42 are rejected by reasoning similar to that used to reject the limitations of claims 1 and 4 above.

Claim 43 recites limitations found in claim 34 and is rejected for similar reasons to those given above for claim 34.

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-11, 22-27, 38, and 44-49 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gupte et al. as applied to claims 1 and 19 above.

Regarding claim 6, Gupte does not expressly teach using a strobe signal in the model to trigger sampling of a strobed output signal and verify the strobed output signal. However, Gupte does disclose a strobe rule which samples selected signals at regular intervals and to compare the sampled values with known good values to verify that the output signal is correct [*"The strobes section specify the appropriate time to capture expected vectors."* (column 8, line 44 – column 9, line 8)]. The strobe rule of Gupte provides the same functionality as the limitations recited in claim 6. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the strobe rule of Gupte to sample strobed output signals in

response to a strobe signal in the model to simplify creating of the reduced model or to better facilitate the design of circuits which always involve strobe signals. Such a modification would preclude the generation of faulty reduced models that fail to properly sample the strobed signals. The combination could be achieved by a rule that defines the relationship between a strobe signal and one or more strobed signals, and the tolerances related to the strobe signal and sampling the strobed signals.

In response, Applicants provide arguments in favor of claims 1 and 19, which have been addressed above.

Regarding claim 7, Gupte does not expressly teach a rule that includes a strobe output signal time window. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would be obvious to a person of ordinary skill in the art at the time of applicant's invention to define a time window within which a change in strobe output signal to match a predetermined strobe output signal value should occur as a tolerance related to the strobe signals.

Regarding claim 8, Gupte does not teach a rule that includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the

time of applicant's invention to define a time window within which a strobed output signal should hold a predetermined strobed output signal value to indicate correct operation as a tolerance related to sampling the strobed signals.

Regarding claim 9, Gupte does not expressly teach a strobed output signal time window that is non-symmetrically disposed about a time when said strobed output signal is sampled. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a time window that is non-symmetrically disposed about a time when said strobed output signal is sampled as a tolerance related to sampling the strobed signals.

Regarding claim 10, Gupte does not expressly teach a settling time window that is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a settling time window that is at least partially surrounded by a settling time window as a tolerance related to sampling the strobed signals.

Regarding claim 11, Gupte does not expressly teach a settling time window that is at least partially surrounded by a settled time window within which said strobed output signal is not

permitted to change. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a settling time window that is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change as a tolerance related to sampling the strobed signals.

Regarding claims 22-27, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claims 6-11. As the invention of Gupte models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the limitations of claims 22-27 are rejected by reasoning similar to that used to reject claims 6-11 above. As Gupte renders each of claims 1 and 6-11 obvious, so does Gupte render obvious the combination of these limitations in claims 22-27.

Claim 44 appears to recite the limitations of claim 8 in independent form and is therefore rejected for rationale similar to that given above for claim 8.

Claims 45 and 46 appear to recite the limitations of claim 7 and are therefore rejected for rationale similar to that given above for claim 7.

Claim 47 appears to recite the limitations of claim 9 and is therefore rejected for rationale similar to that given above for claim 9.

Claim 48 appears to recite the limitations of claim 10 and is therefore rejected for rationale similar to that given above for claim 10.

Claim 49 appears to recite the limitations of claim 11 and is therefore rejected for rationale similar to that given above for claim 11.

Regarding the rejections of claims 44-49, these claims reiterate the individual limitations found in claims 1 and 6-11, although in a different combination. However, as Gupte renders each of claims 1 and 6-11 obvious, so does Gupte render obvious the combination of these limitations in claims 44-49.

Claim 38 recites a combination of limitations found in claims 1, 4, and 6 and are rejected for the same reasons given above for claims 1, 4, and 6. Gupte anticipates the limitations of claims 1 and 4 and renders obvious the limitations of claim 6. A recombination of those limitations would be similarly obvious in view of Gupte.

4. Claims 15, 31, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gupte as applied to claims 1 and 19 above, and further in view of Rostoker et al. US Patent No. 5,544,067 (Rostoker).

Regarding claim 15, Gupte does not expressly teach monitoring output signals other than at sampling points for that output signal. Rostoker teaches monitoring output signals within the circuit diagrams (Fig. 19, references 1910, 1912, 1914, and 1916; column 11, lines 65-67;

column 30, lines 47-60), i.e. monitoring output signals other than at sampling points for the respective output signal. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to combine monitoring output signals within the circuit diagrams as in the invention of Rostoker with the system simulation of Gupte in order to help the user identify and appropriately correct problems in the design [*"Schematic diagram and simulation displays showing those portions of the electronic system and simulated signal patterns which are related to the design rule violations are used to help the user identify and appropriately correct problems in the design."* (Rostoker, column 6, lines 23-29)] The combination could be achieved by a rule which allows the designer to specify monitoring output signals within the subsystem circuit under test, producing output similar to that of Rostoker.

In response, Applicants allege that Gupte fails to teach "recording, in response to a change, input signals..." which has been addressed above. As per Applicants' request, the motivation to combine the Gupte and Rostoker references has been expressly quoted in the rejection.

Applicants further submit that:

> It is noted that the Gupte specifies at column 9, lines 2-8 that "all outputs are assumed to be synchronous and periodical." Thus, Gupte clearly teaches that a cycle-based approach is suggested and being adopted, rather than Applicants' approach where sampling is performed "in response to changes" in the output signals.

The Examiner does not contest Applicants' reading of the Gupte reference, but reiterates that the claim language "recording, in response to a change, input signals..." does not precisely correspond to Applicants' argument. In particular, the claim language does not appear to

exclude a cycle-based approach where recording occurs "in response to a change" in a periodic clock or strobe signal.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 31, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claim 15. As the invention of Gupte models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the limitations of claims 31 are rejected by reasoning similar to that used to reject claim 15 above.

Claim 39 recites a combination of limitations found in claims 1, 4, and 15. Gupte anticipates the limitations of claims 1 and 4 and renders obvious the limitations of claim 15. A different combination of those limitations would be similarly obvious in view of Gupte.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

Paul P. Rodriguez 1/4/06
Primary Examiner
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